Flexible DSP platform for various workload patterns

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ABSTRACT

Future multimedia communication products require system chips that provide sufficient computing capacity and configuration flexibility for achieving interoperability between different communication systems and support for various multimedia signal processing standards. A flexible DSP platform that utilises pre-designed IP cores, such as DSP and RISC processors, advanced coprocessors for critical functions and configurable memory organisation is presented. ADSL, HiperLAN2 subset and MPEG2 decoding algorithms have been analysed as a basis of IHIP architecture design. The initial performance results look promising and it seems that the IP block based configurable architecture could provide satisfactory performance for various types of workloads.

1. INTRODUCTION

Future multimedia products must be capable to provide both high computational capacity and effective execution of different kinds of algorithms and applications. Algorithmic complexity of DSL (digital subscriber line), mobile and wireless communication standards are increasing heavily [1, 2]. Interoperability of different systems, such as UMTS (universal mobile telecommunication system) and WLAN (wireless local area network), and a need to support various compression and source coding standards, such as MPEG4 and MP3, set demanding requirements for processing platforms [3, 4, 5].

Integrated computer systems, e.g. system chips have been the kernels of telecommunication products. Integration capacity of System Chip technology is developing rapidly [6]. The capacity of a single chip doubles in every 18 months according to Moore's law and within next years, tens of complete computer systems can be integrated into a single ASIC. It will mean that a high-performance PC with memories can be scaled down to a single system on chip that has both capabilities to base-band and application processing.

The development of system chips is a huge effort even to best organisations. The reuse of existing designs and procurement of intellectual property make design more effective. The IP (intellectual property) based design requires standardised ways for interconnecting different virtual components [7]. Platform based design have been proposed as a solution for design complexity management [8]. Manufacturing integration platforms provide implemented hardware resources that can be used in the various applications. The application can be designed using hardware or software configuration or both [9].

The research hypothesis in this paper is that by combining ideas from configurable architectures and intellectual property based design it is possible to have effective platform architecture for various types of algorithms and applications. The key issues in the design of flexible DSP platform are the analysis of application characteristics and the evaluation of platform performance.

2. APPLICATION CHARACTERISTICS

There are basically three different categories of signal processing, when using the data timing characteristics for classification: stream, block and sporadic data processing.

In stream based processing, size of incoming data token is usually small (from few bits to few bytes), token arrive periodically or, at leas1t in some degree, predictably. Data is processed in many stages and SAR (segmentation and re-assembly) functions between stages are common. Number of operation for data token in each stage is usually quite small. Streaming data processing is be done most naturally in pipelined processing architecture, because the SAR functions can be implemented in between pipeline stages and pipelining is associated with high data throughput requirements. Due to high throughput requirements, stream based processing requires fast clock speed, small but fast buffer memories between stages and solid method of inter-process or inter-stage synchronisation. Examples of stream based processing in this paper are HiperLAN2 and ADSL base-band processing.

In block based processing data tokens to be processed are large, ranging from hundreds of bytes to thousands or even millions bytes. This causes number of requirements

for processing architecture. Data transfers happen in long bursts with inactivity times in between, which causes requirements for peak bandwidth of buses. Address space, memories, and memory bandwidth must also be large. Block based processing usually allow data parallel processing with MIMD (multiple instructions, multiple data) or SIMD (single instruction, multiple data) type of processors.

In Internet era, a hybrid form of streaming and block based data processing has emerged with the internet protocol based communications. Implementations of physical and data link layer manifest streaming characteristics, but network layer manifests block based processing characteristics with large packet sizes, large memory requirements associated with ordering and error detection codes for whole packet. Therefore current and especially future Internet infrastructure requires programmable signal processing platforms that are well suited for both types of processing.

Most difficult form of data processing is sporadic data processing. Size of data token is predictable but only worst case estimates and some statistics of data arrival rate is known. If hard real-time requirements are associated for this type of data processing, architecture must be designed for the worst case. This however may leave significant resources idle for most of the time. For achieving acceptable power consumption, chip should comprise of several parallel blocks where clocking of unneeded blocks can be switched off. Other solution is the use of adapting clock speed.

1.1. ADSL, HiperLAN2 and MPEG2

Case examples for flexible DSP platform are ADSL and HiperLAN2 processing and MPEG2 video decoding.

Programmable implementation of ADSL remote modem requires approximately 900-1300 MOPS (millions of operations in second) on typical DSP processor with MAC (multiply-accumulate) unit [1].

The estimated resources for HiperLAN2 modem in simplest case (6Mbit/s data-rate, BPSK modulation scheme) are around 600 MOPS for transmitter and 850 MOPS for receiver, excluding the Viterbi-decoding [4].

As block based processing example, MPEG-2 MP@ML video decoding at 30 frames per second sampled in YCrCb 4:2:0 and MP3 audio or MPEG2 audio is considered [5]. The most essential design parameter considering MPEG-2 video decoding is the high memory, memory bus and system bus bandwidth requirements. Raw uncompressed data stream bandwidth is 15 Mbits/s but internal communication results in huge bandwidth requirement. The amount of needed memory is at least 16 Mbit. The required processing resources estimation of the video decoding is estimated to be 620-750 MOPS [10]. This could, however, to be somewhat less since estimates were based on general-purpose processor and the multiplication was estimated to take 4 clock cycles. With VS56000 DSP, multiplication can be done in single clock cycle.

3. IHIP ARCHITECTURE

Case example presented in this paper is the IHIP (information highway interface platform) chip. The IHIP consists of RISC computer that is based on of Leon 32-bit SparcV8 RISC core designed by European Space Agency, and DSP cluster with four VS56000 24-bit fixed point DSPs and Viterbi and FFT coprocessors. The basic architecture is shown in Fig. 1.

In addition IHIP chip has a DMA unit, 16 Mbit on-chip memory and an interface to external bus. Components are connected with 32-bit AMBA (Advanced Microcontroller Bus Architecture) bus that supports pipelining bus accesses, split transactions, burst transactions and multiple bus-masters. Leon core can also access the memory blocks of DSP cluster in some operation modes.

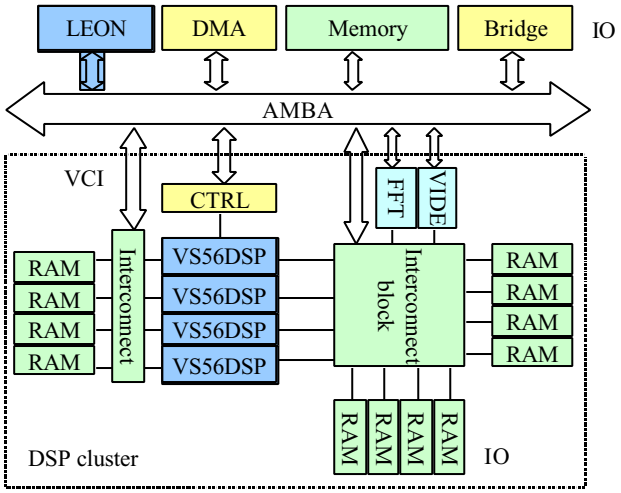

Fig. 1 IHIP Architecture

The components in the chip are introduced into the design as third party IP-blocks (intellectual property). These individual blocks are connected to the system bus via VSIA OCB (on-chip-bus) wrappers so the system bus can be modified or changed if needed without modifying the IP blocks and vice versa [7, 8].

In the DSP-cluster, the cores are connected with a configurable shared memory system (each core can access 64 kwords of memory per bus). There are four memory banks for each X and Y data buses and four 16kword segments in each bank. Each 16kword segment can be mapped to any processor or even for all processors at the same time. All processors can access to same piece of memory when needed or make a pipeline from one processor to another.

Two co-processors are needed in most computing intensive tasks of applications. For ADSL's FFT and IFFT there is an IP-block that can calculate 256-point complex to complex transformations. For the Viterbi-

decoding in HiperLAN2 receiver, there is a dedicated IP block.

The estimated processing capacity of the chip is at GOPS (giga operations per second) range. The chip is targeted to 0.13µm (or even more advanced) CMOS process technology that has ability to implement large on-chip DRAM memories. Target clock frequency is 200 MHz, which would provide 200 MIPS per DSP processor core and 200 MIPS for the Leon RISC core. The main on-chip DRAM memory would be 16Mbit and the used clock frequency would provide a peak bandwidth of 6400 Mbits/s for AMBA bus. The conceptual design and VHDL and SystemC implementation so far has been made without concerning too much on the technology constraints, as the chip is supposed to use future state-of-the-art technology process.

1.2. Configurable memory system

The configurable shared-memory system has three basic configurations, but the architecture allows others too.

- In parallel mode each DSP processor has private data and program memories.
- In pipelined mode memory is configured so that a core feeds a shared memory segment and another reads from the same segment. In Fig. 2, and example of pipeline configuration is shown. DMEM means data memory and PMEM program memory.
- In concurrent mode, common memory banks are mapped for all cores.

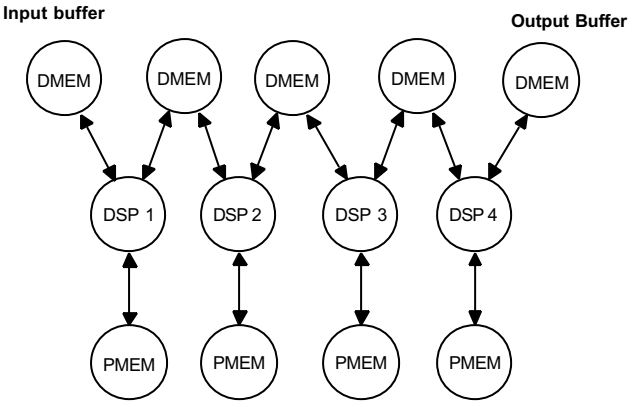

Fig. 2 DSP Cluster in pipeline mode.

Inter-processor synchronisation is achieved by reserving the 64-word peripheral memory area from DSP core's X-bus. These registers are used as semaphores or status registers between DSP cores and the Leon.

1.3. Operation modes and control

The basic idea in the control of IHIP architecture is that the LEON core controls DSP clusters operation, operation mode changes and configuration changes. There are four possible states:

- In the initialization state the basic system checks are performed.
- In operation mode change state the program and data are loaded to DSP cluster and system is configured according to operation mode
- In operation mode data is processed at DSP Cluster and RISC computer. During the operation the configuration of the memory system does not change.
- In configuration change mode, the memory configuration is changed. This used for transferring data between processing units.

The state of DSP cluster is controlled via the status registers and interrupts. The platform control must be explicitly programmed. The benefits are full control over the execution and possibility to fully exploit the capacity of DSP cluster.

1.4. Operation scenarios

In ADSL modem mode, one DSP core acts as transmitter and three DSP cores and RISC core are allocated to receiver side. The FFT block is also required for the receiver. In the receiver side two DSPs handle Reed-Solomon decoding, FFT-block handles fast Fourier transformation and RISC core and the remaining DSP handle the rest of the processing. The shared memory of the DSP cluster and FFT in the receiver side is configured as pipeline to allow easy data transfer and synchronisation between processing stages.

In HiperLAN2 case, two DSP cores are allocated on the transmitter side and two DSP cores, RISC core, FFT-block and Viterbi-decoder are allocated for the receiver side. The processing and memory bandwidth requirements are so high that additional FFT block might be needed, but this is confirmed in further simulations. The shared memory and co-processor blocks are configured as two parallel pipelines, one pipeline consisting of transmitting side DSP cores and possible additional FFT block and the other pipeline consisting of receiver side DSP cores, FFT-block and Viterbi-decoder.

In MPEG2 case DSP cores handle the IDCT (inverse discrete cosine transformation) and the RISC core handles other tasks. The shared memory of the DSP cores is configured as concurrent mode, where all cores can access same data.

4. EVALUATION OF ARCHITECTURE

Initial performance estimations suggest that ADSL and MPEG-2 fit in to the IHIP architecture easily. However if a Reed-Solomon decoder would be implemented as additional IP block it would take 400 MIPS of processing burden off the DSP cores. The HiperLAN2 might need additional FFT block to allow both receiver FFT and transmitter IFFT to be processed in hardware co-processor. These open questions should have an answer after further simulations are done.

The register-based configuration of DSP cores, the DSP shared memory and co-processors is very software friendly and intuitive and the programming of the chip is very similar to a single embedded RISC processor programming. The problematic software development for the DSP cluster is not yet tackled. For the DSP shared memory, the programmable switch matrix approach is proving to be very efficient solution to add flexibility to architecture.

The 16Mbit of on-chip memory is very challenging part of the design, although IBM provides up to 16Mbit of embedded DRAM memory blocks even today [11]. Also the clock frequency of 200 MHz for the DSP cores and the Leon core might not be feasible.

There is also an option of changing the processor cores to achieve better performance. The Leon RISC core could be exchanged for a more state-of-the-art ARM or MIPS processor core and 24-bit VS56000 DSPs could be changed to floating point or 32-bit fixed point cores. The current choice of cores is partly done because of the easy availability of VHDL implementations of the cores.

5. CONCLUSIONS

A flexible DSP platform that utilises pre-designed IP cores, such as DSP and RISC processors, advanced coprocessors for critical functions and configurable memory organisation is presented. The proposed architecture can be configured so that execution of various workload patterns is efficient so that unnecessary on-chip communication load can be minimised. The control solution for DSP cluster and configuration management approach seem to provide good basis for software development.

ADSL, HiperLAN2 subset and MPEG2 decoding algorithms have been analysed as a basis of IHIP architecture design. The initial performance results look promising and it seems that the IP block based configurable architecture could provide satisfactory performance for various types of workloads.

The implementation complexity of IHIP chip has not been studied yet. The next step is to implement development and verification platform for the architecture and to study in detail the operation of architecture and application mapping issues.

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